IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

AXEL HARTWIG ET AL

Serial No.

Filed: CONCURRENTLY

MULTIPROCESSOR ARRAY

Atty. Docket

DE 000167

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

3. (Amended) A multiprocessor array as claimed in claim 1, characterized in that the first clock domain and/or the at least one second clock domain include more than one processor.

4. (Amended) A multiprocessor array as claimed in claim 1, characterized in that in order to read out data from the first shadow register unit (3) and/or the at least one second shadow register unit (11) the multiplexer unit (18) is connected thereto in the read out direction.

5. (Amended) A multiprocessor array as claimed in claim 1, characterized in that requests for access from the first

shadow register unit (3) and/or the at least one second shadow register unit (11) to the priority unit (19) are encoded as a one-bit signal.

6. (Amended) A multiprocessor array as claimed in claim 1, characterized in that the priority unit (19) grants priority to the first shadow register unit (3) or to the at least one second shadow register unit (11) in conformity with the principle: first-come, first-served.

7. (Amended) A multiprocessor array as claimed in claim 1, characterized in that the priority unit (19) grants priority to the first shadow register unit (3) or to the at least one second shadow register unit (11) in conformity with the principle: all shadow register units (3, 11) are served successively.

8. (Amended) A multiprocessor array as claimed in claim 1, characterized in that the priority unit (19) grants priority to the first shadow register unit (3) or to the at least one second shadow register unit (11) in conformity with the principle: each shadow register unit is statistically allocated a given percentage of the time for accessing the peripheral unit (17).

9. (Amended) A multiprocessor array as claimed in claim 1, characterized in that the peripheral unit (17) is constructed as an infrared interface, UART interface or USB interface.

10. (Amended) A multiprocessor array as claimed in claim 1, characterized in that the first shadow register unit (3) and/or the at least one second shadow register unit (11) are connected to the associated processor (2, 10) via an interrupt (8, 16).

11. (Amended) A communication terminal using a multiprocessor array as claimed in claim 1.

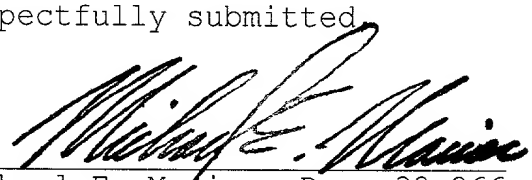
12. (Amended) A portable device using a multiprocessor array as claimed in claim 1.

REMARKS

The foregoing amendments to claims 3-12, were made solely to avoid filing the claims in the multiple dependent form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicant respectfully reserves all rights he may have under the Doctrine of Equivalents. Applicant furthermore reserves his right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

By 
Michael E. Marion, Reg. 32,266
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APPENDIX

3. (Amended) A multiprocessor array as claimed in claim 1 ~~or 2~~, characterized in that the first clock domain and/or the at least one second clock domain include more than one processor.

4. (Amended) A multiprocessor array as claimed in claim 1 ~~one of the preceding claims~~, characterized in that in order to read out data from the first shadow register unit (3) and/or the at least one second shadow register unit (11) the multiplexer unit (18) is connected thereto in the read out direction.

5. (Amended) A multiprocessor array as claimed in claim 1 ~~one of the preceding claims~~, characterized in that requests for access from the first shadow register unit (3) and/or the at least one second shadow register unit (11) to the priority unit (19) are encoded as a one-bit signal.

6. (Amended) A multiprocessor array as claimed in claim 1 ~~one of the preceding claims~~, characterized in that the priority unit (19) grants priority to the first shadow register unit (3) or to the at least one second shadow register unit (11) in conformity with the principle: first-come, first-served.

7. (Amended) A multiprocessor array as claimed in claim ~~1 one of the claims 1 to 5~~, characterized in that the priority unit (19) grants priority to the first shadow register unit (3) or to the at least one second shadow register unit (11) in conformity with the principle: all shadow register units (3, 11) are served successively.

8. (Amended) A multiprocessor array as claimed in claim 1 ~~one of the claims 1 to 5~~, characterized in that the priority unit

(19) grants priority to the first shadow register unit (3) or to the at least one second shadow register unit (11) in conformity with the principle: each shadow register unit is statistically allocated a given percentage of the time for accessing the peripheral unit (17).

9. (Amended) A multiprocessor array as claimed in claim 1 ~~one of the preceding claims~~, characterized in that the peripheral unit (17) is constructed as an infrared interface, UART interface or USB interface.

10. (Amended) A multiprocessor array as claimed in claim 1 ~~one of the preceding claims~~, characterized in that the first shadow register unit (3) and/or the at least one second shadow register unit (11) are connected to the associated processor (2, 10) via an interrupt (8, 16).

11. (Amended) A communication terminal using a multiprocessor array as claimed in claim 1 ~~the preceding claims~~.

12. (Amended) A portable device using a multiprocessor array as claimed in claim 1 ~~the preceding claims~~.